Appl. No. 10/620,743
Examiner: KENNEDY, JENNIFER M, Art Unit 2812
In response to the Office Action dated November 29, 2004

Date: February 22, 2005
Attorney Docket No. 10112491

REMARKS

Applicant thanks the Examiner for indication of allowable subject matter in claims 10-21, and for acknowledging Applicant's claim to foreign priority and receipt of the certified copy of the priority document. Responsive to the Office Action mailed on November 29, 2004 in the above-referenced application, Applicant respectfully requests amendment of the above-identified application in the manner identified above and that the patent be granted in view of the arguments presented. No new matter has been added by this amendment.

Present Status of Application

Claims 1-21 are pending. The disclosure and claims 1, 10 and 21 are objected to because of informalities. Claims 1 and 10 are rejected under 35 U.S.C 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1 and 5-8 are rejected under 35 U.S.C 102(e) as being anticipated by Tews et al (US 6,426,253). Claims 2 and 3 are rejected under 35 U.S.C 103(a) as being unpatentable over Tews et al in view of Kawai et al (US 6,410,991). Claims 4 and 9 are rejected under 35 U.S.C 103(a) as being unpatentable over Tews et al in view of Divakaruni et al (US 2001/0042880). Claims 10-21 are indicated as allowable if rewritten or amended to overcome the rejections under 35 U.S.C 112, second paragraph, set forth in the office action.

In this paper, the specification and claims are amended according to the suggestion of the Examiner to overcome the objections. Claims 1 and 10 are amended according to the suggestion of the Examiner to overcome the rejections under 35 U.S.C. 112, second paragraph. Claim 1 is amended to more clearly identify novel aspects of the invention. Support for the amendments can be found on page 7, lines 21-28 and Figs. 3c-3h of the application.

Reconsideration of this application is respectfully requested in light of the amendments and the remarks contained below.

Allowable Subject Matter

Applicant thanks the Examiner for her indication in the Office Action that claims 10-21 would be allowable if rewritten to overcome the rejections under 35 U.S.C. 112, second paragraph.

Applicant has amended claim 10 according to the suggestion of the Examiner. It is therefore Applicant's belief that claim 10 is in condition for allowance. Insofar as claims 11-21 depend from claim 10, it is Applicant's belief that these claims are also in condition for allowance.

Rejections Under 35 U.S.C. 102(e)

Claims 1 and 5-8 are rejected under 35 U.S.C 102(e) as being anticipated by Tews et al. To the extent that the grounds of the rejections may be applied to the claims now pending in this application, they are respectfully traversed.

Claim 1 has been amended to recite a method for forming a trench capacitor comprising the steps of providing a semiconductor substrate, wherein a deep trench and a deep trench capacitor are formed therein, the deep trench capacitor having a node dielectric layer and a storage node, the node dielectric layer covering a sidewall and a bottom portion between the deep trench and the storage node of the deep trench capacitor, and the storage node filling the deep trench to a predetermined depth; ion implanting the top portion of the deep trench at a predetermined angle to form an ion doped area on a single sidewall of the semiconductor substrate and the top surface of the deep trench capacitor; forming an oxide layer on the ion doped area; forming a sidewall layer on the sidewall of the deep trench using the oxide layer as a mask, wherein the sidewall layer is isolated from the storage node of the deep trench capacitor; removing the oxide layer; forming a barrier layer on the interior of the deep trench and the sidewall layer; and filling a conducting layer in the deep trench.

As shown in Figs. 3c-3h of the application, in a preferred embodiment of the invention, a step of ion implanting the top portion of the deep trench (304) at a predetermined angle is performed to form an ion doped area on a single sidewall (304a) of the semiconductor substrate (301) and the top surface of the deep trench capacitor (307+306+305). An oxide layer (308) is formed on the ion doped area. A sidewall layer (309) is formed on the sidewall of the deep trench (304)

using the oxide layer (308) as a mask, wherein the sidewall layer (309) is isolated from the storage node (307) of the deep trench capacitor (307+306+305). The oxide layer (308) is removed. A barrier layer (310) is formed on the interior of the deep trench (304) and the sidewall layer (309). A conducting layer (312+314) is filled in the deep trench (304).

The present invention thus forms an additional layer (309) on a single sidewall of a top portion of a deep trench (304) to reduce width of the top portion, thereby efficiently isolating adjoining capacitor wires (314).

Tews et al fail to teach or suggest a method for forming a trench capacitor comprising, *inter alia*, the steps of forming a sidewall layer on the sidewall of the deep trench using the oxide layer as a mask, wherein the sidewall layer is isolated from the storage node of the deep trench capacitor, removing the oxide layer, and forming a barrier layer on the interior of the deep trench and the sidewall layer, as recited in claim 1.

MPEP 2131 prescribes that to anticipate a claim, a reference must teach every element of the claim. In this regard, the Federal Circuit has held:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).
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> "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Tews et al teach a method of forming a trench capacitor. As shown in Figs. 4-12 of Tews et al, a low-angle dopant implantation 114 is performed on a polysilicon layer 112 overlying a polysilicon layer 110 (which the Examiner relies upon as teaching the storage node of the trench capacitor recited in claim 1), creating a doped and an undoped polysilicon layer 120 in a trench. See Fig. 4. By performing thermal oxidation and partial etching, an oxide layer 122 is left on a

portion of the trench surface and the undoped polysilicon layer 120 is exposed. See Figs. 5-6. Using the oxide layer 122 as an etching mask, the undoped polysilicon layer 120 and a portion of the polysilicon layer 110 are removed to form a recessed trench (124+126) exposing a portion of the polysilicon layer 110. See Figs. 7-8. A polysilicon layer 130 (which the Examiner relies upon as the sidewall layer recited in claim 1) electrically connecting the polysilicon layer 110 to a terminal of the vertical trench transistor is deposited in the recessed trench (124+126). See Fig. 9. By performing oxidation and oxide-etching, the excess polysilicon layer 130 is then removed to form a remaining polysilicon layer serving as a buried strap 142, as shown in Figs. 10-12. An insulating layer (136+138) is formed on the trench surface. A conductor 140 fills the trench. See Fig. 12.

Applicant notes that in Tews et al, the polysilicon layer 130 serves as a buried strap 142 electrically connected to the polysilicon layer 110. In contrast, claim 1 recites forming a sidewall layer on the sidewall of the deep trench using the oxide layer as a mask, wherein the sidewall layer is isolated from the storage node of the deep trench capacitor.

Applicant therefore submits that Tews et al do not teach or suggest forming a sidewall layer on the sidewall of the deep trench using the oxide layer as a mask, wherein the sidewall layer is isolated from the storage node of the deep trench capacitor; removing the oxide layer; and forming a barrier layer on the interior of the deep trench and the sidewall layer. For at least this reason, it is Applicant's belief that claim 1 is allowable over the cited reference. Insofar as claims 2-9 depend from claim 1, it is Applicant's belief that these claims are also in condition for allowance.

Rejections Under 35 U.S.C. 103(a)

Claims 2 and 3 are rejected under 35 U.S.C 103(a) as being unpatentable over Tews et al in view of Kawai et al. Claims 4 and 9 are rejected under 35 U.S.C 103(a) as being unpatentable over Tews et al in view of Divakaruni et al.

As noted above, it is Applicant's belief that that claims 2-4 and 9 are allowable by virtue of their dependency from claim 1. For this reason, the Examiner's arguments in connection with these claims are considered moot and will not be addressed here.

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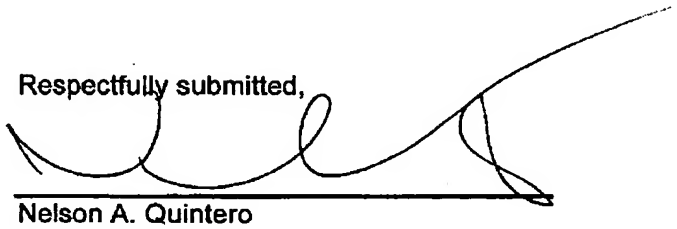
Conclusion

The Applicant believes that the application is now in condition for allowance and respectfully requests so.

Respectfully submitted,



Nelson A. Quintero
Reg. No. 52,143
Customer No. 34,283
Telephone: (310) 401-6180

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